Isetta 6502 cycles 20231128

		Addressing mode						
	LD/ST			zp,x		abs,x		
	Isetta, 6502	imm	zp	zp,y	abs	abs,y	(ind,x)	(ind),y
	LDA	3, 2	4, 3	5, 4	5, 4	6, 4	9, 6	9, 5
	LDX, LDY	4, 2	5, 3	6, 4	6, 4	7, 4		
	STA		3, 3	4, 4	4, 4	5, 5	8, 6	8, 6
	STX, STY		4, 3	5, 4	5, 4			

		Addressing mode							
	Arithmetic				zp,x		abs,x		
	Isetta, 6502	implied	imm	zp	zp,y	abs	abs,y	(ind,x)	(ind),y
	INC			5, 5	6, 6	6, 6	7, 7		
	INX, INY	4, 2							
	DEC			5, 5	6, 6	6, 6	7, 7		
	DEX, DEY	4, 2							
	ADC		4, 2	5, 3	6, 4	6, 4	7, 4	10, 6	10, 5
	SBC		4, 2	5, 3	6, 4	6, 4	7, 4	10, 6	10, 5
	CMP		3, 2	4, 3	5, 4	5, 4	6, 4	9, 6	9, 5
	CPX, CPY		4, 2	5, 3		6, 4			

		Addressing mode							
	Logic / Shift				zp,x		abs,x		
	Isetta, 6502	acc	imm	zp	zp,y	abs	abs,y	(ind,x)	(ind),y
	AND		3, 2	4, 3	5, 4	5, 4	6, 4	9, 6	9, 5
	ORA		3, 2	4, 3	5, 4	5, 4	6, 4	9, 6	9, 5
	EOR		3, 2	4, 3	5, 4	5, 4	6, 4	9, 6	9, 5
	BIT			9, 3		10, 4			
	ASL	4, 2		5, 5	6, 6	6, 6	7, 7		
	LSR	4, 2		8, 5	9, 6	10, 6	11, 7		
	ROL	4, 2		5, 5	6, 6	6, 6	7, 7		
	ROR	5, 2		10, 5	11, 6	11, 6	12, 7		

TAX, TAY	3, 2
TXA, TYA, TXS	3, 2
TSX	4, 2
PHA	6, 3
PLA	7, 4
PHP	12, 3
PLP	11, 4
CLC	2, 2
SEC	2, 2
CLV	3, 2

	Program flow		uncond	uncond	condition	condition	condition
	Isetta, 6502	implied	abs	indirect	EQ or NE	VS or VC	other
	JMP		6, 3	7, 5			
	Bcc				4/8, 2	TBD, 2	3/7, 2
	JSR		18, 6				
	RTS	8, 6					
	NOP	2, 2					